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## Back junction n-type silicon heterojunction solar cells with $V_2O_5$ hole-selective contact

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### Abstract

In this work, a back junction solar cell design is explored for n-type crystalline silicon by using thermally evaporated  $V_2O_5$  as a rear hole contact and  $n^+$  amorphous silicon (a-Si:H) as a front electron contact. Photoconductance measurements revealed an implicit open-circuit voltage ( $i-V_{OC}$ ) of 670 mV for the solar cell precursor (before metallization), achieved by maximizing the work function of  $V_2O_5$  with a thin nickel capping layer. The  $V_{OC}$  value of the finished device was lower than projected at 617 mV, most likely due to poor passivation of the active area perimeter. Nonetheless, an efficiency of 14.2% was achieved (in polished substrates), proving the potential of such a novel structure.

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**Keywords:** Silicon heterojunction solar cell; Hole-selective contact; Transition metal oxide; Vanadium pentoxide

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### 1. Introduction

During the past decades, crystalline silicon (c-Si) has become the dominant photovoltaic technology due to its well-known device physics and high throughput processing. However, further lowering of its production cost depends on the implementation of novel processes and materials with lower energy budget. In parallel, the development of organic photovoltaics has introduced a great number of hole- and electron-selective materials whose

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optoelectronic properties are comparable or superior to the conventional p- and n-doped layers used in c-Si (either thermally-diffused homojunctions or heterojunctions based on hydrogenated amorphous silicon, a-Si:H). Recent research involving the use of such “alternative” materials on c-Si includes the formation of thin (<20 nm) hole-selective layers with thermally-evaporated transition metal oxides MoO<sub>3</sub>, WO<sub>3</sub> and V<sub>2</sub>O<sub>5</sub> [1,2,3,4], working as front-side emitters in n-type crystalline silicon (n-Si) and as back-surface fields in p-type crystalline silicon (p-Si) solar cells [4], with a proven record conversion efficiency of 22.5% [5]. Given their high work function values (> 5 eV), these materials are capable of inducing either an inversion layer on n-Si or an accumulation layer on p-Si, working as contacts that extract photogenerated holes. When used as front emitters, their wide energy bandgap ( $E_{\text{gap}} > 3$  eV) reduces the absorption losses of the device by  $\geq 1$  mA/cm<sup>2</sup> when compared to front emitters based on a-Si:H ( $E_{\text{gap}} \sim 1.7$  eV). However, the main advantage of these materials is their ambient temperature and/or solution-based processing.

Despite these benefits, transition metal oxides are known for their sensitivity to air exposure, drastically lowering their work function [6] and/or degrading their passivation potential. Further passivation losses occur by ion-bombardment and UV-luminescence when transparent electrodes of indium-tin oxide (ITO) are sputtered over these oxides [2,5], a necessary step due to their poor conductivity ( $\sim 10^{-6}$  S/cm). Moreover, post-processing of the device (for example, post-fabrication annealing) is limited to temperatures below 130 °C [5,7], because of thermal instabilities of the oxide or its interface with c-Si or ITO. To overcome these problems, this work reports on a back junction n-Si solar cell with V<sub>2</sub>O<sub>5</sub> (work function  $\Phi_{\text{V}_2\text{O}_5} \sim 6.7$  eV,  $E_{\text{gap}} \sim 2.8$  eV) acting as hole-selective contact. Passivation losses caused by air exposure are avoided by a 20 nm Ni capping layer ( $\Phi_{\text{Ni}} \sim 5$  eV), while damage caused by ITO sputtering is prevented by directly contacting with an Al back electrode. These modifications allow to fully take advantage of the passivation potential of V<sub>2</sub>O<sub>5</sub>, measured as an implicit open-circuit voltage ( $i$ - $V_{\text{OC}}$ ) of 678 mV, demonstrating its feasibility as a hole contact in back junction architectures.

## 2. Device structure and fabrication

The back junction n-Si/V<sub>2</sub>O<sub>5</sub> solar cells were fabricated on FZ (100 orientation, 280 μm thickness) wafers with 2.7 Ωcm resistivity. After standard RCA cleaning, samples were dipped in 1% HF (1 min) and washed with deionized water. A stack of intrinsic (5 nm) and n<sup>+</sup>-doped (15 nm) a-Si:H layers was deposited on the front side by Plasma Enhanced Chemical Vapor Deposition (PECVD), resulting in a passivated electron-selective contact (or front surface field). After a brief air exposure, an 80 nm 120 Ω/sq ITO film was sputtered (RF-magnetron) as a front anti-reflection conductive layer. At this point, an annealing step at 160 °C was applied for 20 min under a N<sub>2</sub> atmosphere to improve the conductivity of the ITO and recover the passivation quality of the i/n<sup>+</sup> a-Si:H stack after the sputtering process [8]. Regarding the rear side, a 10 nm V<sub>2</sub>O<sub>5</sub> film (99.99%, powdered) was deposited by vacuum thermal evaporation ( $< 8 \times 10^{-6}$  mbar) from a tantalum boat at  $\sim 0.1$  Å/s, comprising the hole-selective contact (or emitter) of the device. Without interrupting the vacuum, a 20 nm Ni capping layer was evaporated from an alumina-coated tungsten boat. After characterizing the device precursor by quasi-steady state photoconductance (QSSPC) measurements, a 300 nm Al layer was evaporated as a rear electrode. Both the rear and front active areas (1 cm<sup>2</sup>) were defined by photolithography, completed by wet etching of the Al/Ni/V<sub>2</sub>O<sub>5</sub> layers and by wet/dry etching of the ITO/n<sup>+</sup> a-Si:H layers. The solar cell was finalized by an evaporated Ag front grid (3 μm, 4.3% shadow), as depicted in figure 1(a) with its fabrication steps.

As for the front junction device, the fabrication process has been described elsewhere [3] and mainly differs from the back junction process in (1) the rear i/n<sup>+</sup> a-Si:H stack is capped by an 80 nm a-SiC<sub>x</sub> rear reflector and contacts the c-Si substrate by laser firing, followed by annealing at 160 °C/20 min; (2) after a brief air exposure (< 5 min) of the V<sub>2</sub>O<sub>5</sub> layer, ITO is sputtered; (3) the active front area (1 cm<sup>2</sup>) is defined by photolithography while the rear contact (full area) consists of thermally evaporated Al. Figure 1(b) depicts the front junction solar cell structure and its main fabrication steps.

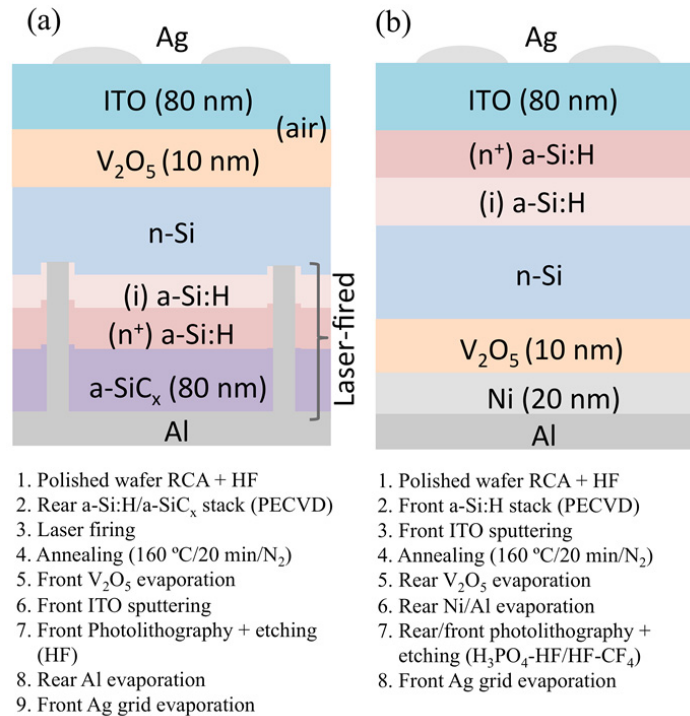


Fig. 1. Schematic of the n-type c-Si/V<sub>2</sub>O<sub>5</sub> front (a) and back (b) junction solar cells, along with main processing steps.

### 3. Device characterization

Figure 2 shows the QSSPC measurements of the n-Si/V<sub>2</sub>O<sub>5</sub> front (1) and back (2) junction device precursors (before Al metallization and active area defining). For the back junction, an implicit open-circuit voltage ( $iV_{OC}$ , 1 sun intensity) of 670 mV is measured (equivalent to a dark saturation current  $J_0 \sim 85$  fA/cm<sup>2</sup>), while the front junction shows a lower value of 644 mV ( $J_0 \sim 205$  fA/cm<sup>2</sup>) before ITO sputtering. The difference between both values could be attributed to work function lowering of the air-exposed V<sub>2</sub>O<sub>5</sub> from  $\sim 6.7$  to  $\sim 5.7$  eV [6]. Additionally, a fraction of  $iV_{OC}$  loss is also due to the passivation damage induced by the laser firing of the rear a-Si:H/a-SiCx stack. Furthermore, the potential  $V_{OC}$  of the front junction degrades to 619 mV after the ITO sputtering process, a loss that could be partially recovered by low temperature annealing (160 °C/20 min) at the expense of a Fill Factor loss of 20%, as previously reported in [7]. This recovery in passivation suggests that even though annealing improves the n-Si/V<sub>2</sub>O<sub>5</sub> interface, it permanently deteriorates the V<sub>2</sub>O<sub>5</sub> layer or its interface with ITO. Therefore, the potential of a V<sub>2</sub>O<sub>5</sub> hole-selective contact is higher when a thin metallic layer keeps it from reacting to redox environments and when the device is not subjected to straining post-processing steps. This last condition limits the applicability of V<sub>2</sub>O<sub>5</sub> to standard solar cell processing unless moderate temperature steps ( $T > 100$  °C) are bypassed or performed before its deposition.

In order to determine the optimal potential of the n-Si/V<sub>2</sub>O<sub>5</sub> junction, a reference structure was also fabricated using an i/n<sup>+</sup> a-Si:H/a-SiCx stack on the opposite side that provides an excellent passivation quality ( $\tau_{eff\ stack} \sim 1.3$  ms). As shown in figure 2, this structure (3) had an  $iV_{OC}$  of 678 mV, very close to the maximum open-circuit voltage that could be achieved with this n-Si/V<sub>2</sub>O<sub>5</sub> heterojunction. Since the a-Si:H/a-SiCx stack has a surface recombination velocity  $S_{stack} \sim 20$  cm/s (as previously obtained by QSSPC), an emitter saturation current density  $J_{0\ V2O5} \sim 55$  fA/cm<sup>2</sup> is calculated. This value is quite significant considering the dissimilar nature of the heterojunction, the thinness of the oxide layer and the lack of any additional passivation interlayers (such as a-Si:H). Similar results were obtained for the back junction concept reported in [9] for n-Si/PEDOT:PSS, and proves the high-efficiency potential of this structure.

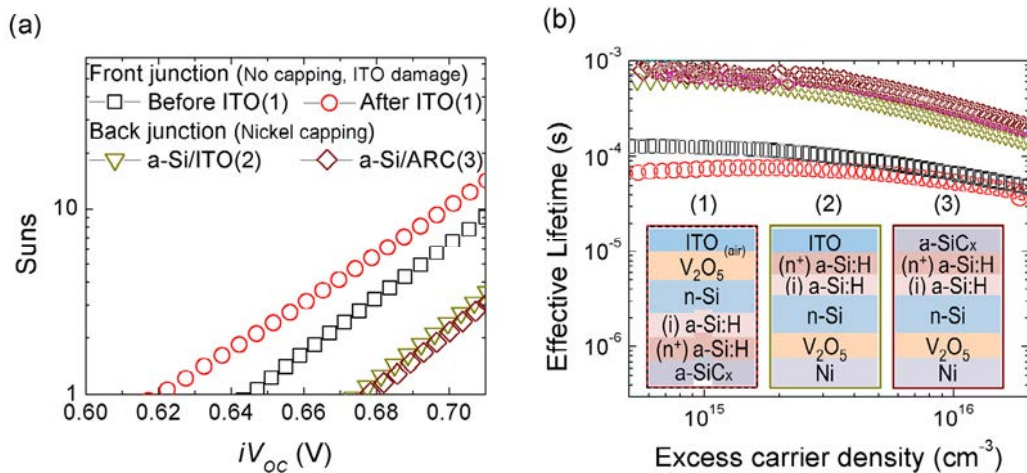


Fig. 2. (a) Implicit open-circuit voltage ( $iV_{OC}$ ) and (b) effective carrier lifetime for the n-Si/V<sub>2</sub>O<sub>5</sub> front (1) and back (2)(3) junctions.

Figure 3(a) shows the current density-voltage ( $J$ - $V$ ) characteristics of the polished substrate solar cells measured under dark and AM1.5g standard illumination at 25 °C, while Table I summarizes the relevant cell performance parameters. Even though the back junction QSSPC results pointed to a larger open-circuit voltage, the measured  $V_{OC}$  was 617 mV, very similar to the front junction  $V_{OC}$  (615 mV). One possible reason for the ~50 mV difference between the QSSPC and  $V_{OC}$  values may be an inaccurate alignment of the top and bottom active cell areas defined during photolithography. Such a misalignment would result on a small but highly recombinative fraction of surface included in the 1 cm<sup>2</sup> photoactive area. This alignment is not critical in a front junction design with a full area rear contact, but it becomes very important in back junctions where the collection of photogenerated carriers occurs on a restricted-area front electrode. Some other reasons for the loss in  $V_{OC}$  could be lateral damage of the front a-Si:H stack during its dry etching with CF<sub>4</sub>, or lack of uniformity of the V<sub>2</sub>O<sub>5</sub>/Ni layers causing a direct contact between Al and n-Si.

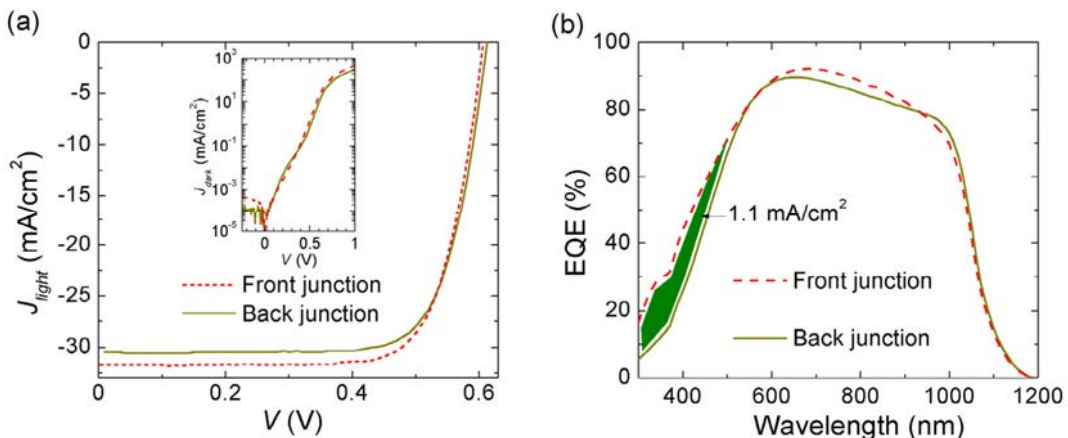


Fig. 3. (a) Current density-voltage ( $J$ - $V$ ) characteristic of the n-Si/V<sub>2</sub>O<sub>5</sub> front and back junction solar cells under standard illumination. Inset shows  $J$ - $V$  under dark conditions. (b) External Quantum Efficiency (EQE) of both devices.

Table 1. Solar cell performance parameters measured at 1.5AMg standard illumination and 25 °C.

V <sub>2</sub> O <sub>5</sub> /n-Si junction solar cell	V <sub>oc</sub> (mV)	J <sub>sc</sub> (mA/cm <sup>2</sup> )	FF (%)	Efficiency (%)
Front-junction	615	31.8	75.1	14.7
Back junction	617	30.4	75.3	14.2

In terms of short-circuit current ( $J_{sc}$ ), the front junction (31.8 mA/cm<sup>2</sup>) clearly outperforms the back junction design (30.4 mA/cm<sup>2</sup>) due to the lower absorption losses of V<sub>2</sub>O<sub>5</sub> compared to the a-Si:H. In Figure 2(b) an evidently higher External Quantum Efficiency response is observed for the front junction device in the short wavelength range (300 – 600 nm), equivalent to 1.1 mA/cm<sup>2</sup>. Despite its  $J_{sc}$  losses, the back junction concept could be useful in interdigitated back-contact designs where front parasitic absorption is minimized by window materials with higher transparency than the a-Si:H/ITO stack used in this work. Finally, it is worth noting that the Fill Factor (FF) of both junctions is fairly equivalent, suggesting that the contact resistivities of both the V<sub>2</sub>O<sub>5</sub>/Ni and V<sub>2</sub>O<sub>5</sub>/ITO contacts are similar and do not depend strongly on the work function differences  $\Phi_{Ni} - \Phi_{V_2O_5}$  and  $\Phi_{ITO} - \Phi_{V_2O_5}$ .

#### 4. Conclusions

In summary, V<sub>2</sub>O<sub>5</sub> was tested as a hole-selective contact for n-type c-Si in a back junction structure, showing a potential  $V_{oc}$  of 678 mV could be achieved when appropriate capping and no ITO sputtering damage is present. Even though the final back junction device could only achieve 617 mV in  $V_{oc}$ , a relatively good Fill Factor of 75% was obtained, indicating the feasibility of a low resistive V<sub>2</sub>O<sub>5</sub>/Ni hole-selective contact. By solving the issues related to  $iV_{oc}$  loss surrounding the back and front active cell areas and by maximizing light absorption (i.e. using a texturized substrate), conversion efficiencies above 18% could be reached for this back junction concept.

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